BOOSTXL-DRV8305EVM User's Guide

This document is provided with the BOOSTXL-DRV8305EVM customer evaluation module (EVM) as a supplement to the DRV8305 data sheet (*DRV8305 Three Phase Gate Driver With Current Shunt Amplifiers and Voltage Regulator*). This user's guide provides details on the setup and hardware implementation of the BoosterPack™ plug-in module.

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Trademarks

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1 BOOSTXL-DRV8305EVM

1.1 PCB 3-D Views

Figure 1 shows the top view of the BOOSTXL-DRV8305EVM board. Figure 2 shows the BoosterPack header signals.

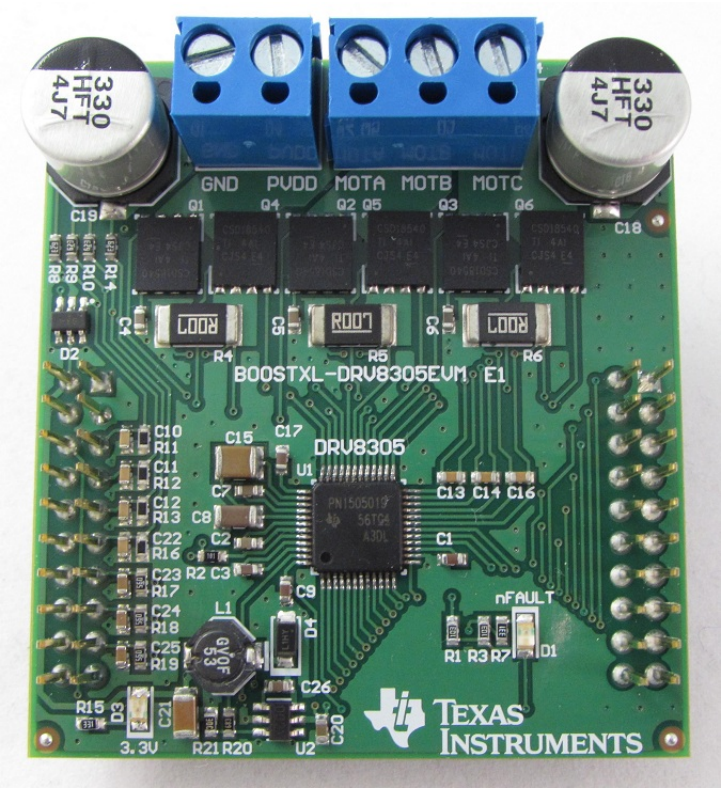

Figure 1. PCB Image (From Above)

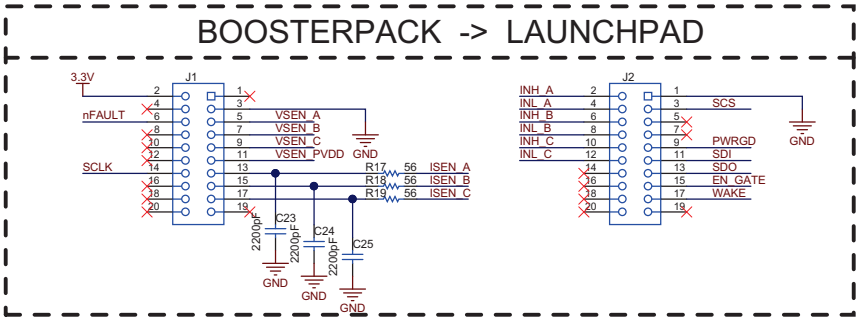

Figure 2. BoosterPack Header Signals

1.2 PCB 3-D Views

Figure 3 and Figure 4 show the top and bottom three-dimensional PCB views.

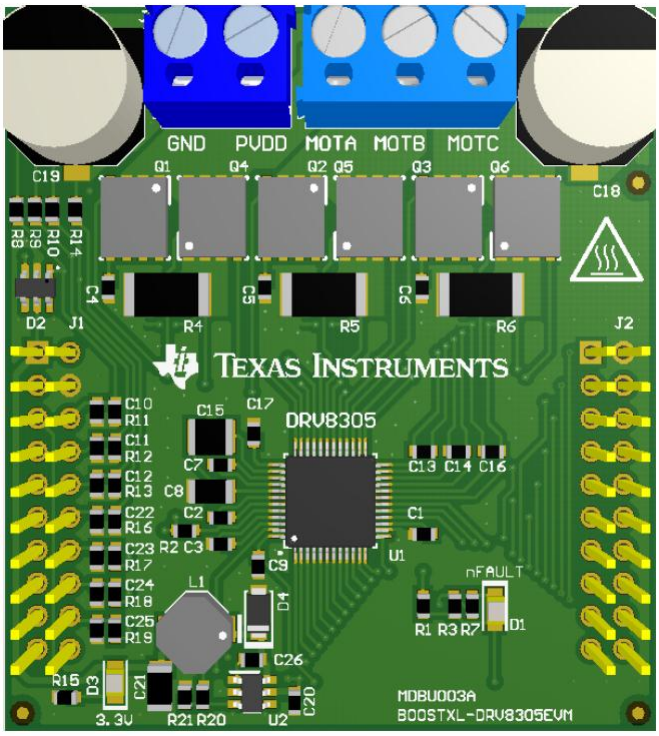

Figure 3. 3-D Top View

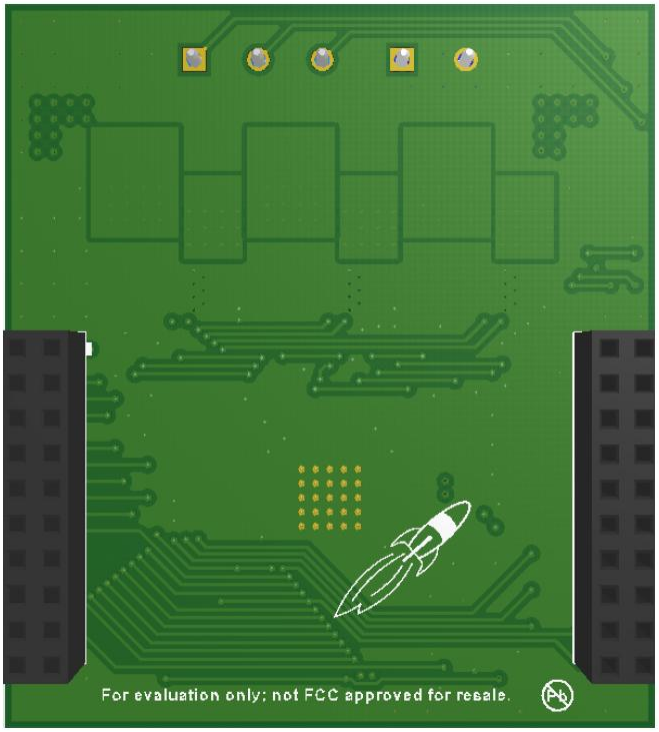

Figure 4. 3-D Bottom View

2 Introduction

The BOOSTXL-DRV8305EVM BoosterPack is a complete 3-phase driver stage in order to evaluate motor application with the DRV8305 motor gate driver. It utilizes a compact and modular form factor for ease of use and is designed to dock with compatible TI LaunchPad™ development kits for a complete motor control system.

2.1 Features

The following lists the BOOSTXL-DRV8305EVM features:

- Complete 3-phase drive stage in a compact form factor (2.0 in × 2.2 in)
- Supports 4.4- to 45-V voltage supply and up to 15-A RMS (20-A peak) drive current
- 6x CSD18540Q5B N-Channel NexFET™ Power MOSFETs (1.8 mΩ)
- Individual motor phase and DC bus voltage sense
- Low-side current shunt sense for each half-bridge
- Fully protected drive stage including short circuit, thermal, shoot-through, and undervoltage protection
- LMR16006 wide voltage input, 0.6-A step down buck regulator for MCU supply
- Combine with compatible LaunchPad XL kits to create a complete 3-phase motor control platform
- Optimized for the Piccolo™ LAUNCHXL-F28027F LaunchPad to support the InstaSPIN-FOC™ sensorless motor control solution

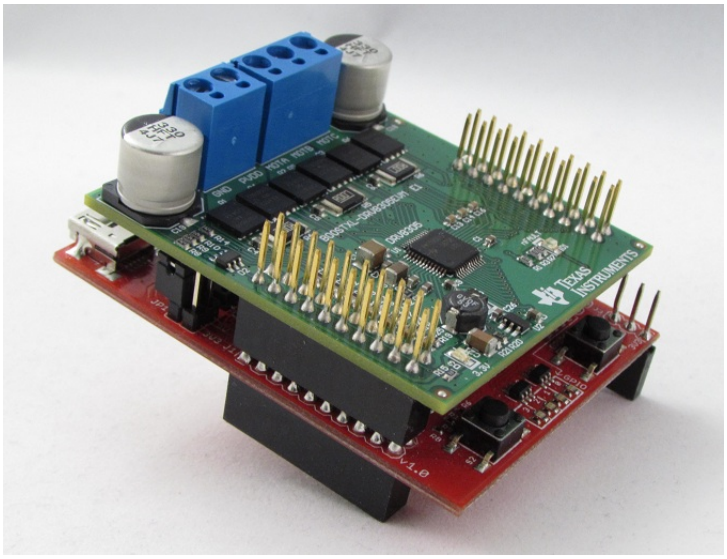

Figure 5. BOOSTXL-DRV8305EVM With LAUNCHXL-F28027F

2.2 Pinout

The BOOSTXL-DRV8305EVM brings out a mixture of power, control, and feedback signals to the XL LaunchPad headers.

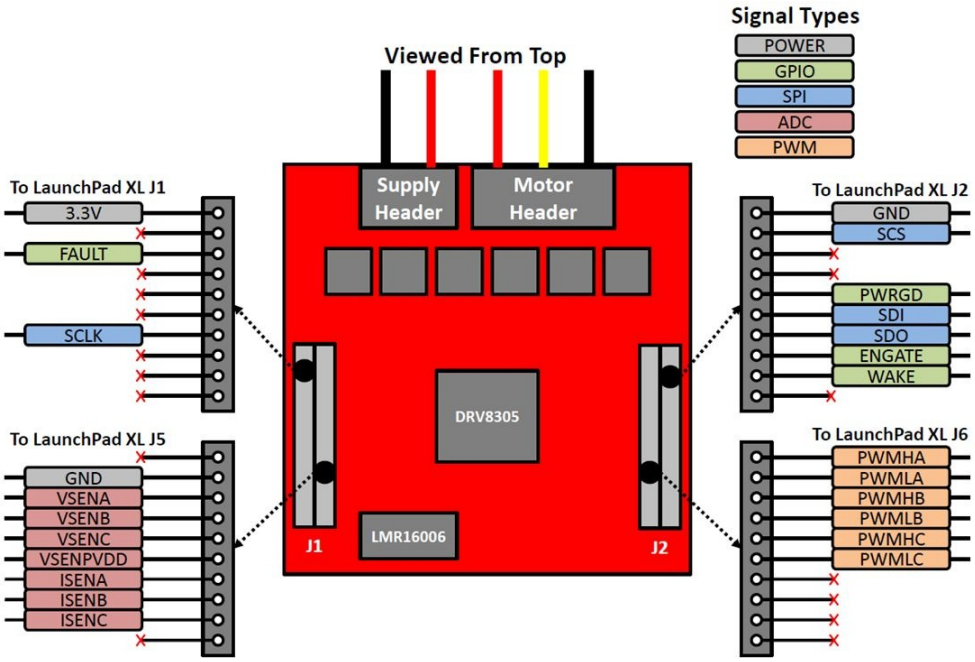

Figure 6. BOOSTXL-DRV8305EVM Pinout

- Terminal block headers for the power supply and motor connections
- Onboard LM16006 step-down buck regulator to provide 3.3-V power to the LaunchPad
- Fault reporting through the nFAULT and PWRGD signals
- SPI to set device configuration, operating parameters, and read out diagnostic information
- Voltage sense for the voltage supply bus and each phase output (scaled for 4.4- to 45-V operation)
- Low-side current shunt sensing on each phase (scaled for 0- to 20-A peak current operation)

2.3 Operating Conditions

Table 1 lists the operating conditions.

Table 1. Operating Conditions

Parameter	Minimum	Maximum	Unit
Operating supply voltage	4.4	45	V
Operating supply current (EN_GATE = Low)		150	mA
Operating temperature	–40	125	°C

3 Getting Started

3.1 Requirements

The BOOSTXL-DRV8305EVM is not a standalone motor control kit and requires a compatible XL LaunchPad to provide the appropriate motor control signals. The BOOSTXL-DRV8305EVM has been specifically designed for the LAUNCHXL-F28027F InstaSPIN-FOC LaunchPad. In addition to the BoosterPack and a compatible XL LaunchPad, a 3-phase motor and sufficient power supply are required.

3.2 Configuring the LaunchPad

The BOOSTXL-DRV8305EVM BoosterPack supplies 3.3 V to the LaunchPad through the onboard LMR16006 0.6-A, step-down buck regulator. It is recommended to remove the jumpers on the LaunchPad that connect the emulation and controller power supplies. The LaunchPad communication lines should also be configured to ensure proper operation from the host PC.

Example: LAUNCHXL-F28027F

For the LAUNCHXL-F28027F LaunchPad, remove the JP1 (3.3 V), JP2 (GND), and JP3 (5 V) jumpers to isolate the two power supply domains (MCU and Emulator).

The S1 switch should be set to the ON-ON-ON position to allow for a JTAG debug connection. The S4 switch should be moved to the OFF position to allow for the nFAULT pin from the DRV8305 to report correctly.

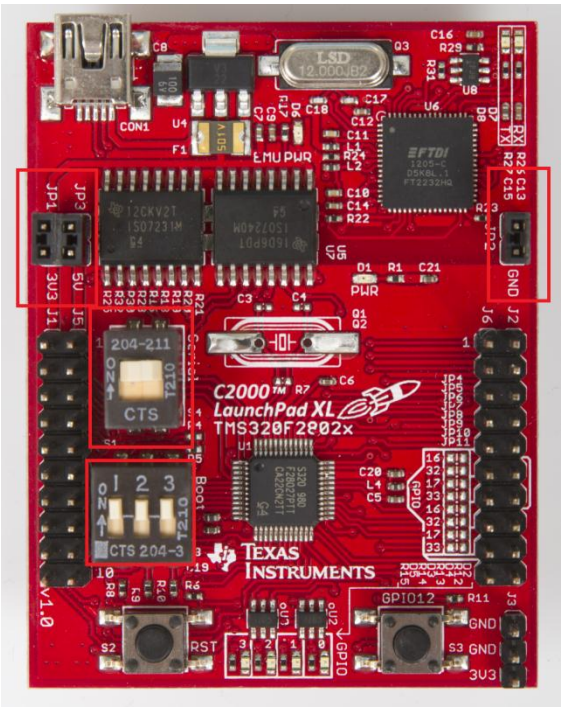

Figure 7. LAUNCHXL-F28027F Configuration

3.3 Connecting the Hardware

Use the following steps to connect the hardware:

1. Plug the BOOSTXL-DRV8305EVM BoosterPack onto the LaunchPad as shown in Figure 5. The terminal block headers should be oriented towards the USB connector and the 20-pin headers (J1 and J2) should align properly.
2. Connect the 3-phase motor to the terminal block header J4. The motor connections have been labeled with A, B, and C but can be connected in any order.
3. Connect the power supply, that will power the BoosterPack's DRV8305 3-phase gate driver, 3-phase power stage, and LMR16006 buck regulator to the terminal block header J3. The connections have been labeled PVDD and GND. For full performance, ensure the supply can support as much current as your motor may demand. The BoosterPack has a designed operating range from 4.4- to 45-V with up to 15-A RMS (20-A peak) of phase output current.

WARNING

At high currents the drive stage can increase to high temperatures. Use proper handling procedures.

4. Enable the power supply. A fault may appear on the nFAULT LED. This is normal and should be cleared when the status registers are read or EN_GATE is taken HIGH.
5. Enable the control algorithm and begin spinning the motor. The BOOSTXL-DRV8305EVM BoosterPack combined with a compatible XL LaunchPad will provide a complete motor drive and control evaluation platform. With the Piccolo LAUNCHXL-F28027F LaunchPad you can take full advantage of **TI's InstaSPIN™-FOC sensorless control solution**. To get started with InstaSPIN-FOC (http://www.ti.com/instaspin-foc) download and run the MotorWare™ software (http://www.ti.com/tool/motorware), reviewing the LAUNCHXL and BOOSTXL resources.

4 Demo Application

The BOOSTXL-DRV8305EVM BoosterPack has been optimized to work together with the Piccolo LAUNCHXL-F28027F LaunchPad to provide a complete motor drive and control evaluation platform. To quickly get your 3-phase motor spinning, see TI's InstaSPIN-FOC sensorless control solution at http://www.ti.com/tool/motorware. Multiple projects, labs, and an easy to use GUI are available with TI MotorWare available at http://www.ti.com/tool/motorware, with detailed documentation and user guides.

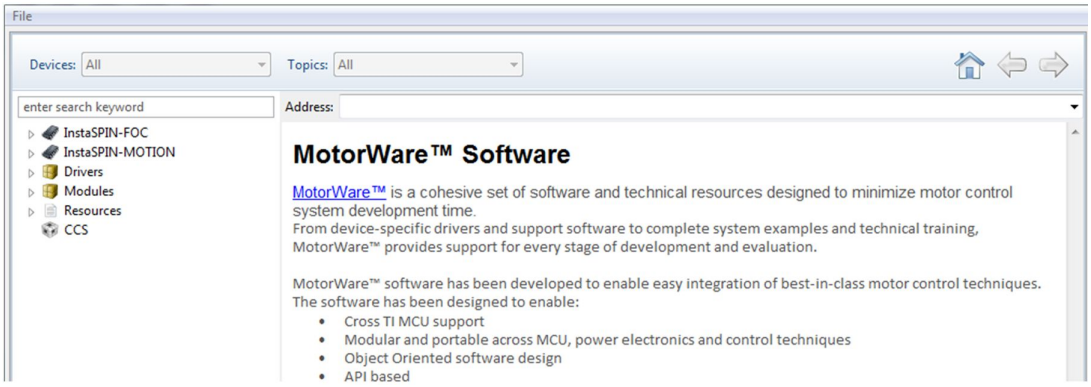

Figure 8. MotorWare™ Software

5 Detailed Hardware Description

The BOOSTXL-DRV8305EVM BoosterPack is a complete drive stage for 3-phase motor applications. The design consists of the DRV8305 motor gate driver, CSD18540Q5B N-Channel NexFET Power MOSFETs, and LMR16006 buck regulator. See the respective data sheets for the DRV8305 (SLVSCX2), CSD18540Q5B (SLPS488), and LMR16006 (SNVSA24) for more information concerning each device.

5.1 DC Bus and Phase Voltage Sense

The BoosterPack has been designed with voltage sense circuits on the DC bus (PVDD) and each half-bridge outputs (phases A, B, and C). These circuits, shown Figure 9, consist of a voltage divider with a filtering capacitor to reduce high frequency noise on the ADC pins. These circuits have been scaled to support 4.4 to 45 V. The high-side resistors for the phase outputs are located near the motor output header (J4) while the low-side resistors and filtering capacitors are located near the ADC pins on the BoosterPack to LaunchPad header (J1) for improved noise reduction purposes.

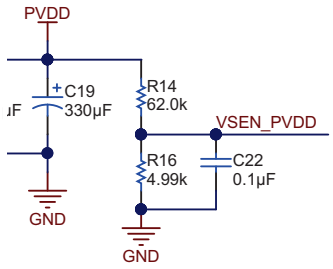

Figure 9. Voltage Sense

To achieve higher resolution voltage feedback, the scaling can be adjusted by replacing the high-side resistors with a lower value.

Example: For a 12-V system, R8, R9, R10, and R14 could be replaced with 22-kΩ resistors to approximately triple the voltage resolution. The new full scale voltage would be 17.85 V.

5.2 Low-Side Current Shunt Sense

The BoosterPack has low-side current shunt sense for each half-bridge (phases A, B, and C). The current sense setup takes advantage of the DRV8305's triple shunt current amplifiers (phases A, B, and c). The configuration for the low-side sense is shown in Figure 9. The differential amplifier senses voltage across a 0.007-Ω power sense resistor with differential connections. The differential voltage is then amplified by 10 V/V and centered at 1.65 V to allow for sensing both positive and negative currents. The sense resistor has been scaled for 0- to 20-A peak currents.

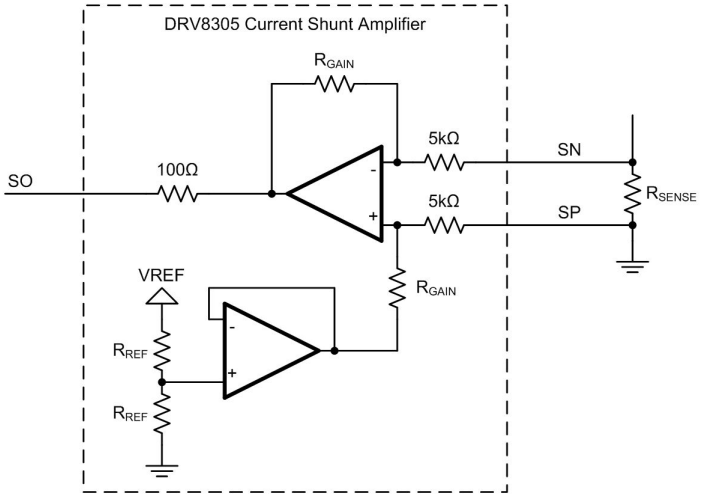

Figure 10. Current Sense

5.3 BoosterPack GPIO Signals

The Motor Drive BoosterPack brings out the GPIO signals for the DRV8301 to the LaunchPad XL. These signals are described in detail in the following list and further information can be found in the DRV8301 data sheet.

1. **nFAULT:** Fault indicator, specific FAULT status can be obtained through the status registers
2. **PWRGD:** Watchdog and LDO regulator status indicator
3. **EN_GATE:** Enables gate driver and current shunt amplifiers
4. **WAKE:** Used to bring the device out of its low power sleep mode.

5.4 DRV8305 Status and Control Registers

The DRV8305 provides extensive fault reporting and device configuration through an SPI interface and internal registers. There are two categories of registers: status and control. Status registers provide information about device faults and warnings. This information can include items ranging from IC overtemperature to MOSFET overcurrent events. The control registers allow various device parameters to be modified to suit system requirements. These parameters include but are not limited to gate drive current, dead times, current shunt amplifier configurations, and fault reporting modes. For specific information concerning the DRV8305 registers, refer to the data sheet (SLVSCX2).

The InstaSPIN GUI allows easy access to read and modify the DRV8305's internal registers. These can be accessed on the DRV8305 tab of the InstaSPIN Universal GUI.

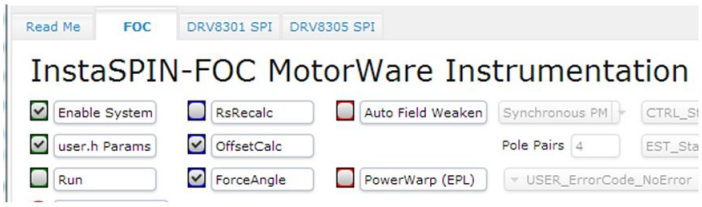

Figure 11. Enable System

Power to the BoosterPack needs to be supplied and **Enable System** needs to be checked to allow SPI reads and writes. The DRV8305 SPI tab displays a map of the DRV8305 internal registers, both status and control. To read from the registers, select the **Read** button. The register map will update with the current register values. To write to the registers, make the desired change in the map and select the **Write** button. Manual reads or writes to individual registers can be made with the **Manual Write** and **Manual Read** buttons (in decimal).

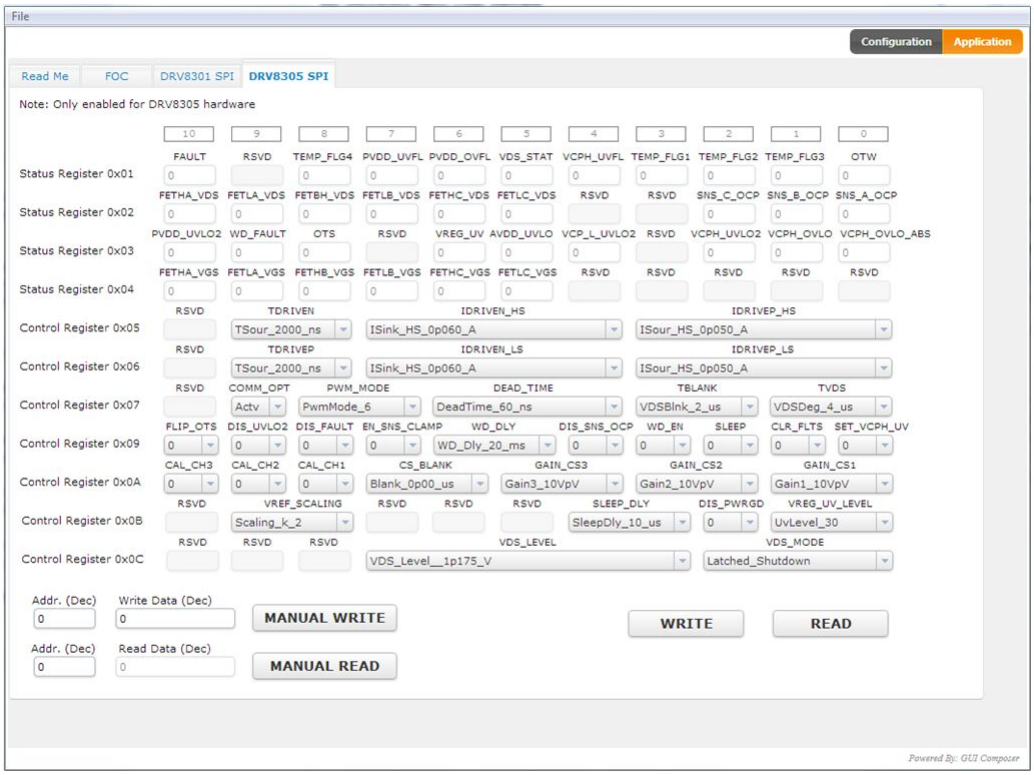

Figure 12. DRV8305 SPI Registers

5.5 BOOSTXL-DRV8305EVM Schematic

Figure 13 shows the BOOSTXL-DRV8305EVM schematic.

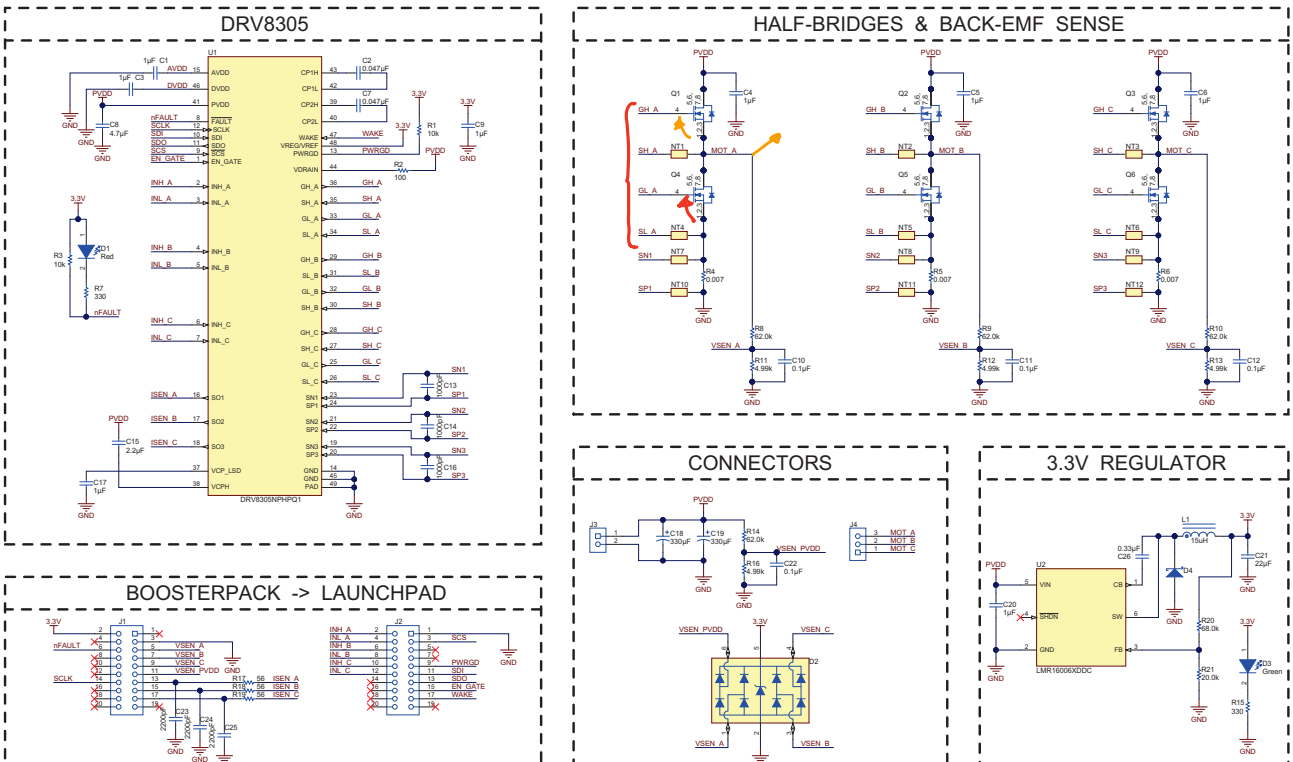

Figure 13. BOOSTXL-DRV8305EVM Schematic

5.6 Hardware Source Files

The complete design files can be found on the tool folder, including the schematic, Gerbers, designs files, PCB views, and bill of materials.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2015) to A Revision	Page
• Added the *Operating Conditions* section	5

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

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      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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CSD18540Q5B 60-V, N-Channel NexFET™ Power MOSFETs

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

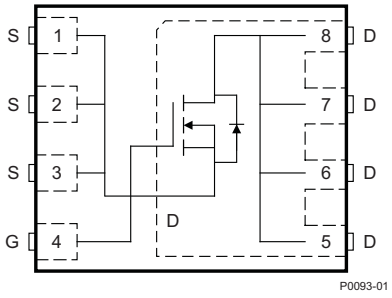
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

3 Description

This 1.8-mΩ, 60-V NexFET™ power MOSFET is designed to minimize losses in power conversion applications with a SON 5-mm × 6-mm package.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	41		nC
Q_{gd}	Gate Charge Gate-to-Drain	6.7		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	2.6	mΩ
		V_{GS} = 10 V	1.8	
$V_{GS(th)}$	Threshold Voltage	1.9		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18540Q5B	2500	13-Inch Reel	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel
CSD18540Q5BT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

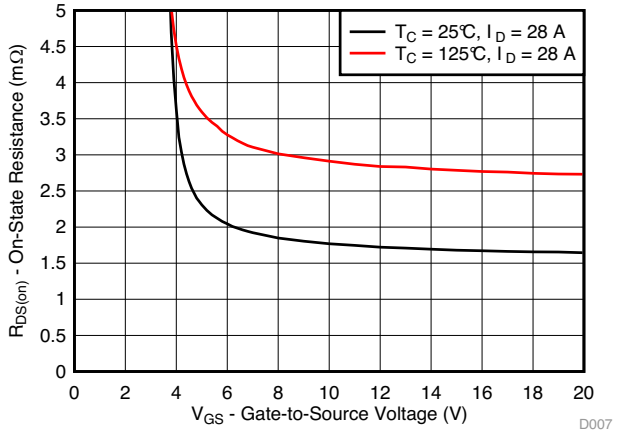
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	205	
	Continuous Drain Current(1)	29	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	400	A
P_D	Power Dissipation(1)	3.8	W
	Power Dissipation, T_C = 25°C	188	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 175	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 80 A, L = 0.1 mH, R_G = 25 Ω	320	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-in², 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.

$R_{DS(on)}$ vs V_{GS}



Gate Charge

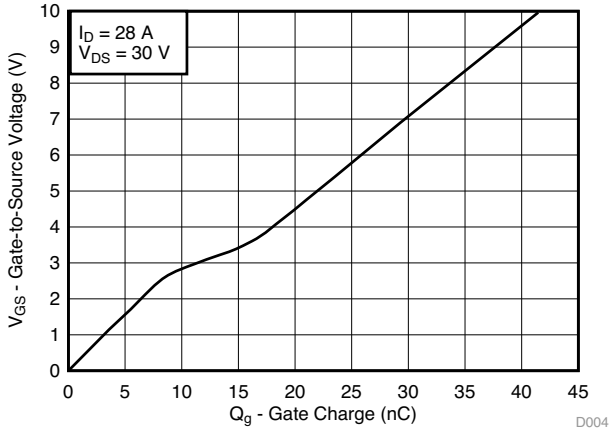


Table of Contents

4 Revision History

Changes from Revision A (June 2016) to Revision B **Page**

- Corrected package size typo in the *Description* section ... 1

Changes from Original (June 2014) to Revision A **Page**

- Updated I_D values. ... 1
- Updated P_D values. ... 1
- Increased maximum temperature to 175°C. ... 1
- Updated Figure 2. ... 5
- Changed Figure 6 to extend temperature to 175°C. ... 5
- Changed Figure 8 to extend temperature to 175°C. ... 6
- Replotted Figure 10 using 175°C data. ... 6
- Changed Figure 12 to extend temperature to 175°C. ... 6
- Added *Receiving Notification of Documentation Updates* and *Community Resources* to *Device and Documentation Support* section. ... 7
- Updated the mechanical drawing. ... 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

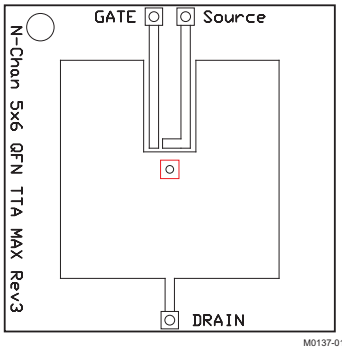
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I = 250 µA	1.5	1.9	2.3	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 4.5 V, I_D = 28 A		2.6	3.3	mΩ
		V_{GS} = 10 V, I_D = 28 A		1.8	2.2	
g_{fs}	Transconductance	V_{DS} = 6 V, I_D = 28 A		116		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		3250	4230	pF
C_{oss}	Output capacitance			622	808	pF
C_{rss}	Reverse transfer capacitance			15	20	pF
R_G	Series gate resistance			0.8	1.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 30 V, I_{DD} = 28 A		20	26	nC
Q_g	Gate charge total (10 V)			41	53	nC
Q_{gd}	Gate charge gate-to-drain			6.7		nC
Q_{gs}	Gate charge gate-to-source			8.8		nC
$Q_{g(th)}$	Gate charge at V_{th}			6.3		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		83		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 28 A, R_G = 0 Ω		6		ns
t_r	Rise time			9		ns
$t_{d(off)}$	Turnoff delay time			20		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 28 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 30 V, I_F = 28 A, di/dt = 300 A/µs		145		nC
t_{rr}	Reverse recovery time			82		ns

5.2 Thermal Information

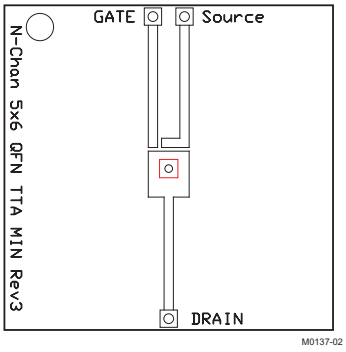
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			0.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

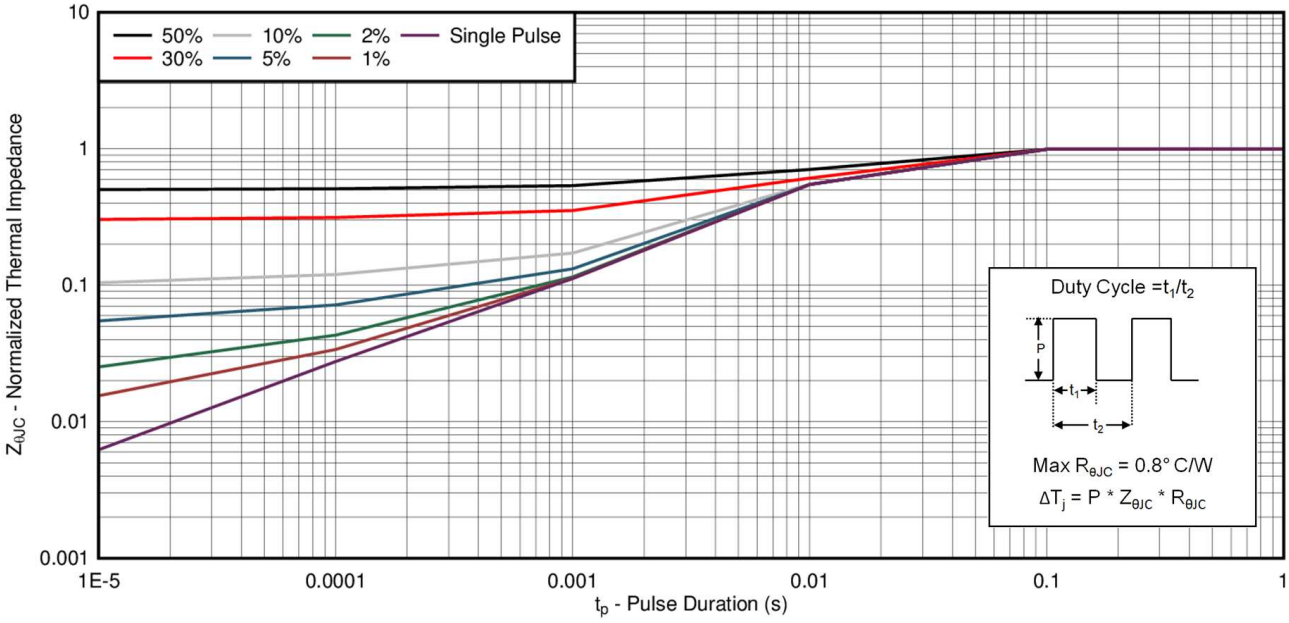


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

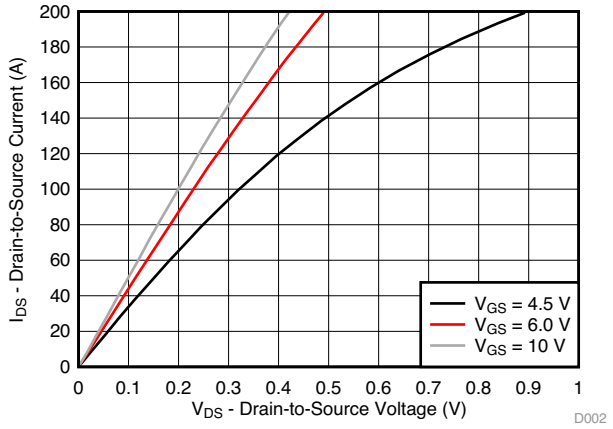


Figure 2. Saturation Characteristics

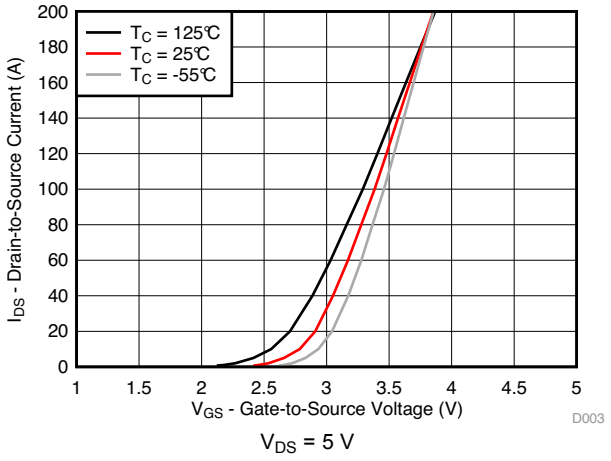


Figure 3. Transfer Characteristics

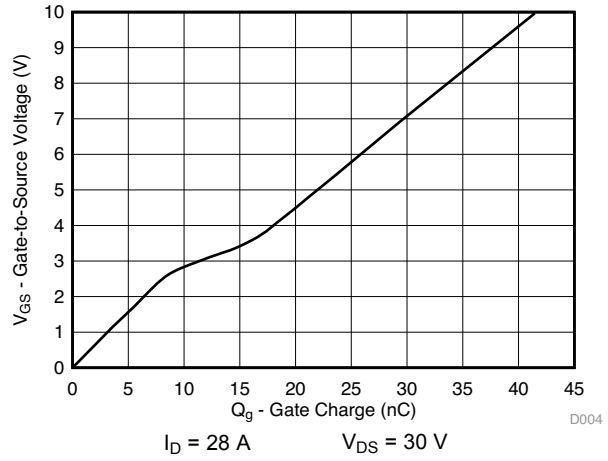


Figure 4. Gate Charge

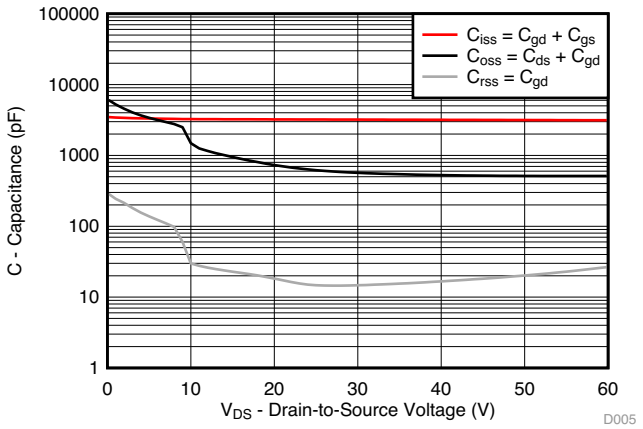


Figure 5. Capacitance

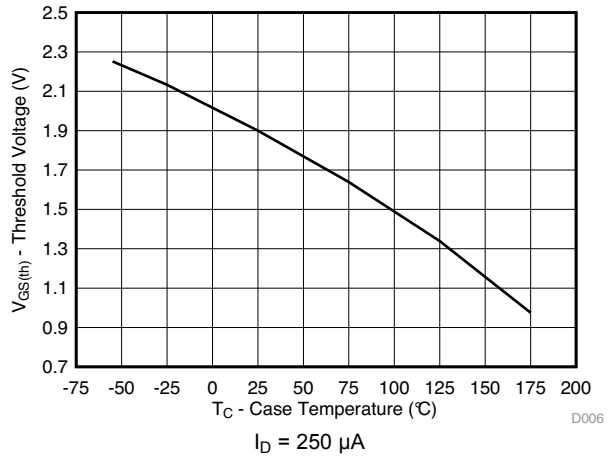


Figure 6. Threshold Voltage vs Temperature

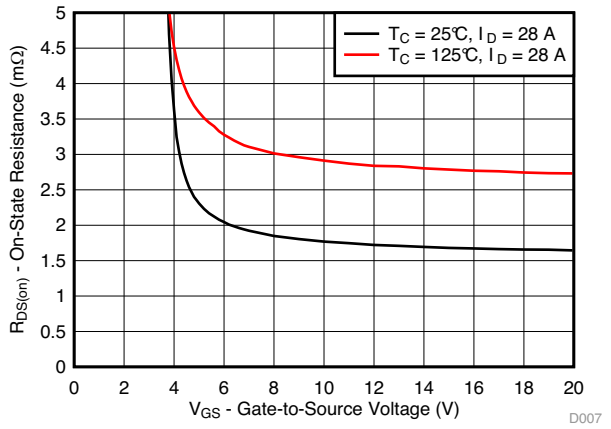


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

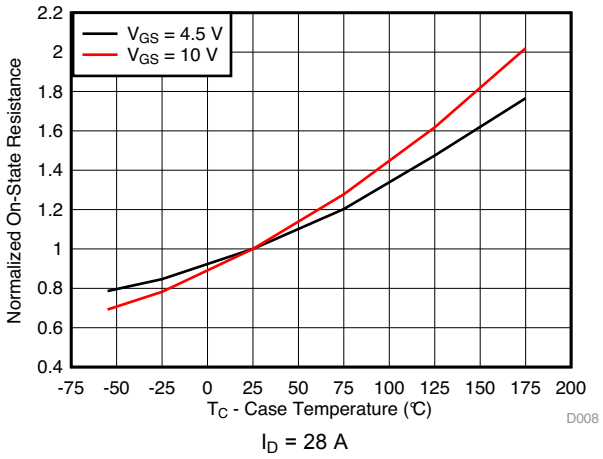


Figure 8. Normalized On-State Resistance vs Temperature

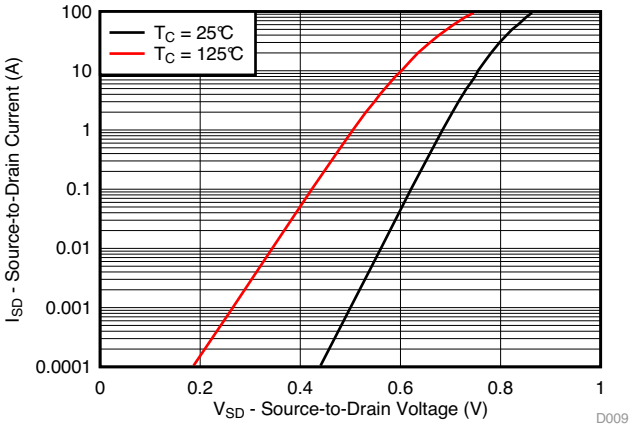


Figure 9. Typical Diode Forward Voltage

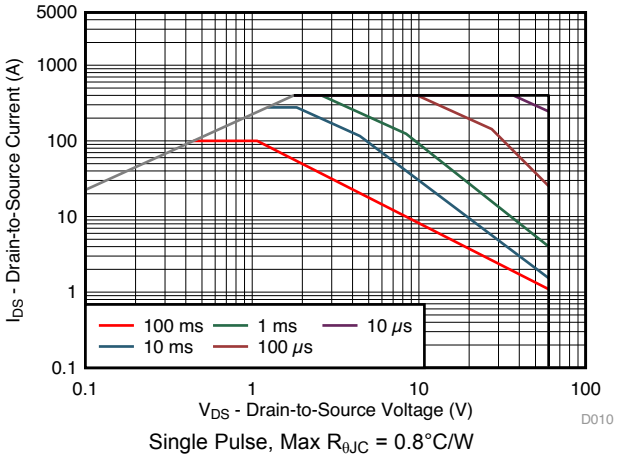


Figure 10. Maximum Safe Operating Area

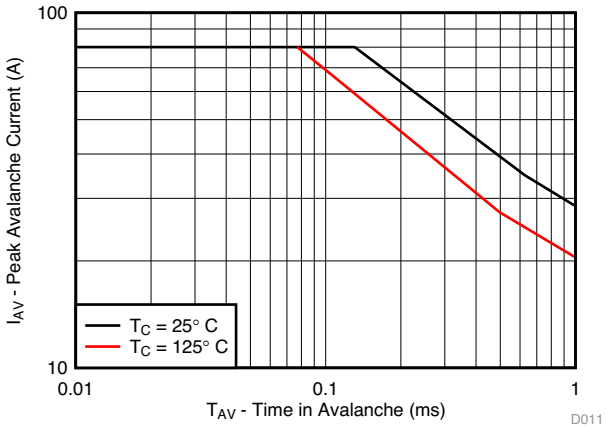


Figure 11. Single Pulse Unclamped Inductive Switching

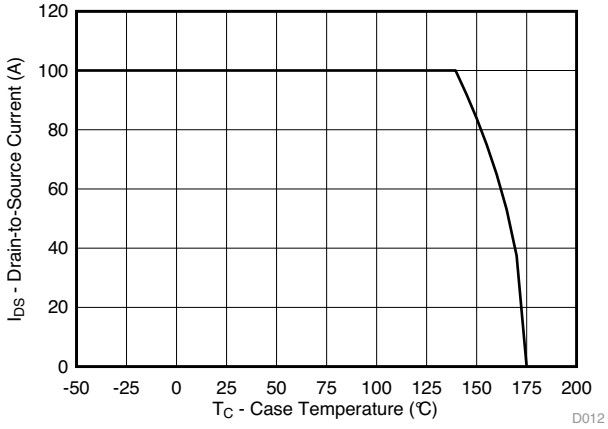


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

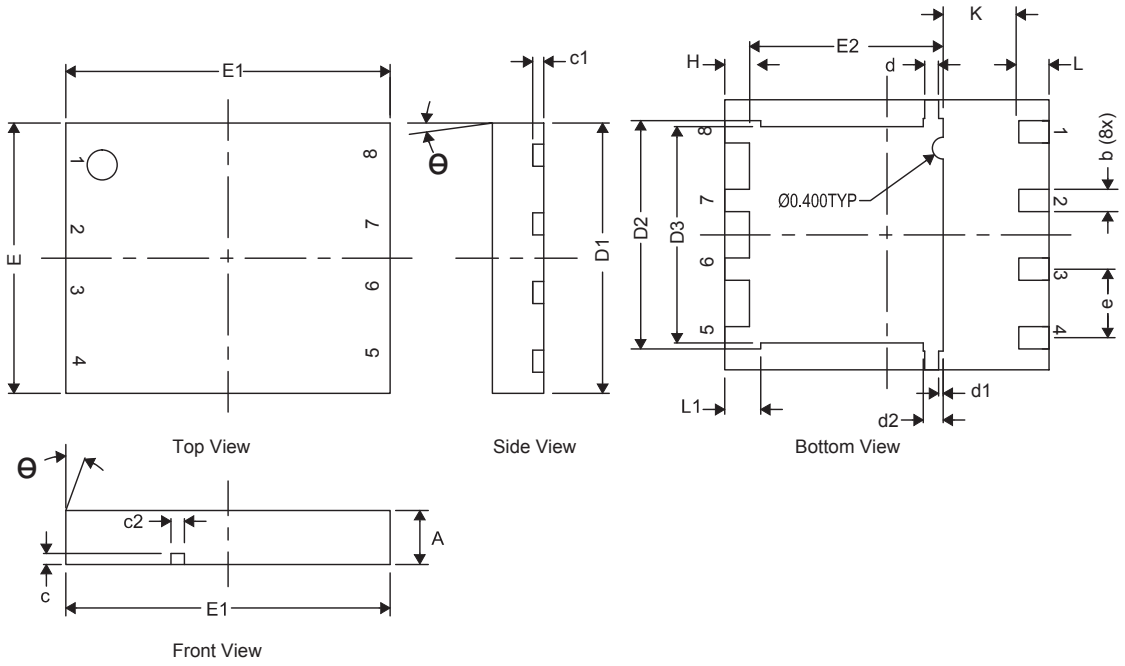
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

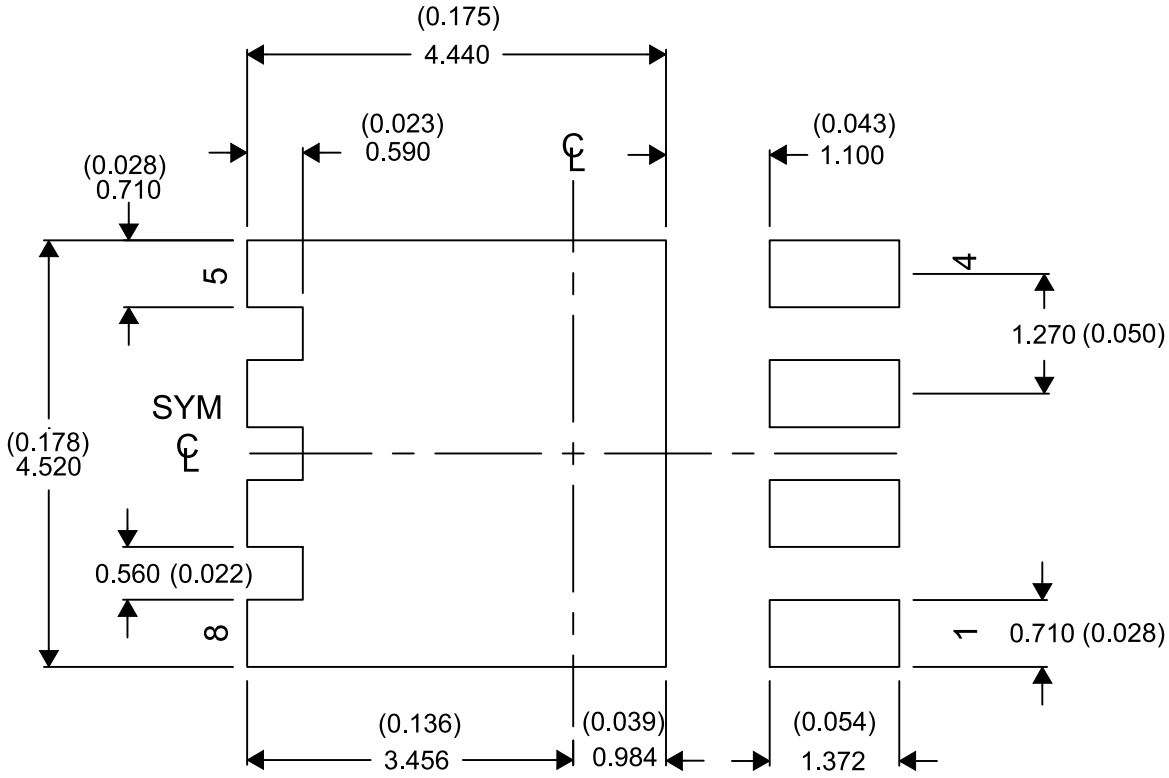
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5B Package Dimensions



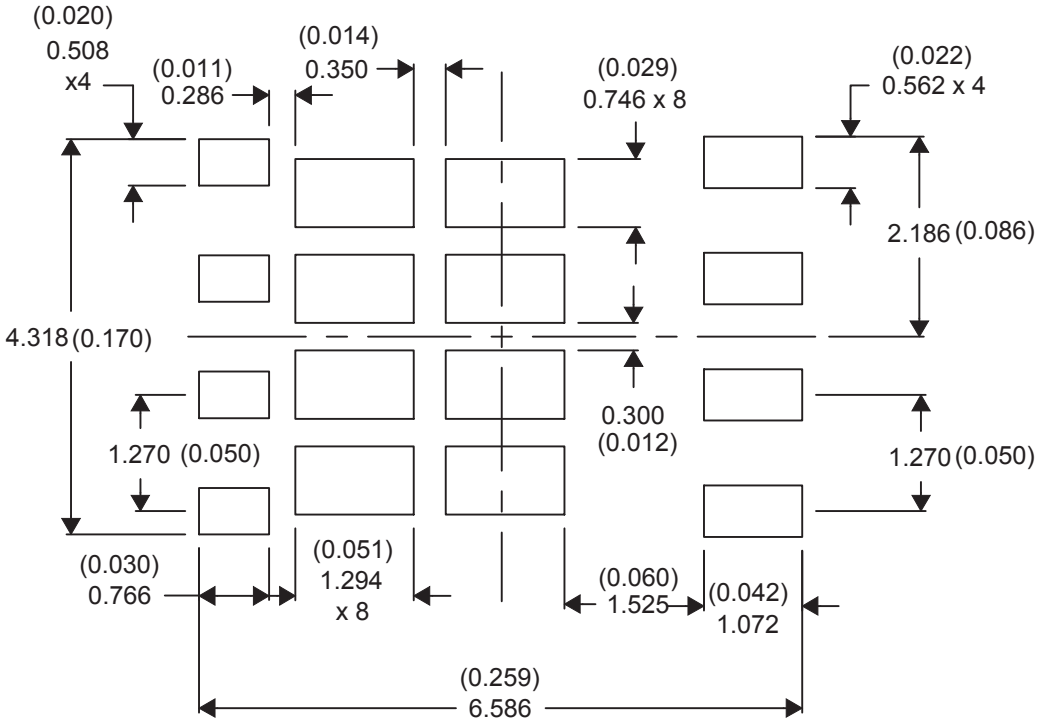
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1		0.085 TYP	
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e		1.27 TYP	
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K		1.40 TYP	

7.2 Recommended PCB Pattern

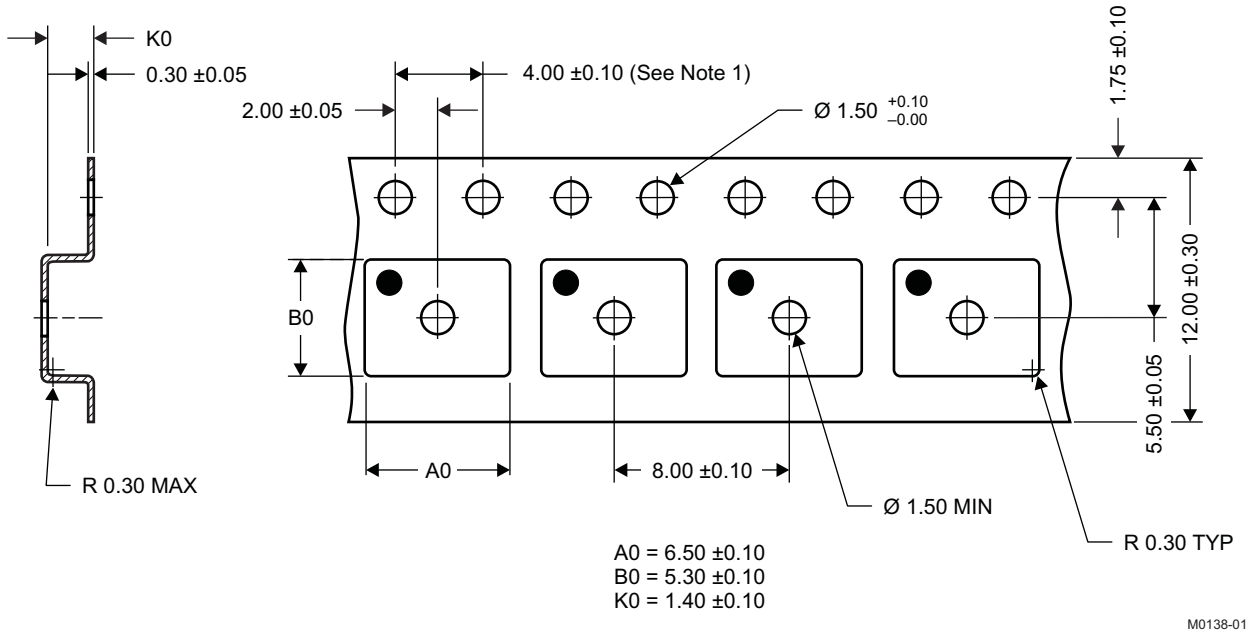


For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Pattern



7.4 Q5B Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18540Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	RoHS-Exempt & Green	NIPDAU I SN	Level-1-260C-UNLIM	-55 to 175	CSD18540	Samples
CSD18540Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	RoHS-Exempt & Green	NIPDAU I SN	Level-1-260C-UNLIM	-55 to 175	CSD18540	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency ECO Mode

1 Features

- Ultra Low 28 µA Standby Current in ECO Mode
- Input Voltage Range 4 V to 60 V
- 1 µA Shutdown Current
- High Duty Cycle Operation Supported
- Output Current up to 600 mA
- 0.7 MHz and 2.1 MHz Switching Frequency
- Internal Compensation
- High Voltage Enable Input
- Internal Soft Start
- Over Current Protection
- Over Temperature Protection
- Small Overall Solution Size (SOT-6L Package)
- Create a Custom Design Using the LMR16006 with the WEBENCH Power Designer

2 Applications

- Industrial Distributed Power Systems
- Automotive
- Battery Powered Equipment
- Portable Handheld Instruments
- Portable Media Players

3 Description

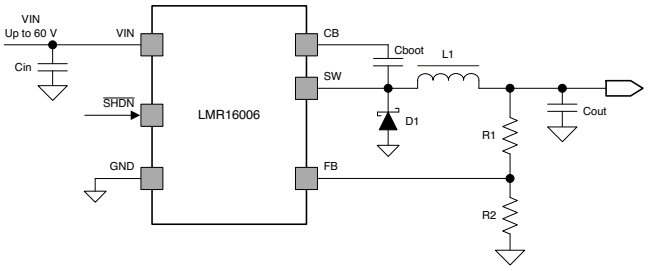
The LMR16006 is a PWM DC/DC buck (step-down) regulator. With a wide input range of 4 V to 60 V, it is suitable for a wide range of application from industrial to automotive for power conditioning from an unregulated source. The regulator's standby current is 28 µA in ECO mode, which is suitable for battery operating systems. An ultra low 1 µA shutdown current can further prolong battery life. Operating frequency is fixed at 0.7 MHz (X version) and 2.1 MHz (Y version) allowing the use of small external components while still being able to have low output ripple voltage. Soft-start and compensation circuits are implemented internally, which allows the device to be used with minimized external components. The LMR16006 is optimized for up to 600 mA load currents. It has a 0.765 V typical feedback voltage. The device has built-in protection features such as pulse by pulse current limit, thermal sensing and shutdown due to excessive power dissipation. The LMR16006 is available in a low profile SOT-6L package.

Device Information(1)

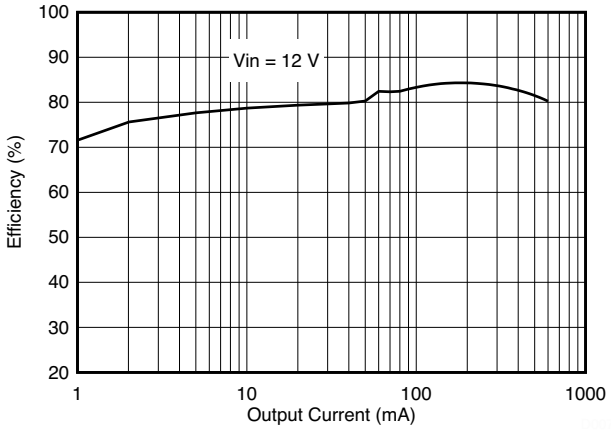
PART NUMBER	PACKAGE	BODY SIZE
LMR16006	SOT (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency vs Output Current (f_{SW}= 0.7 MHz, V_{OUT}= 3.3 V)



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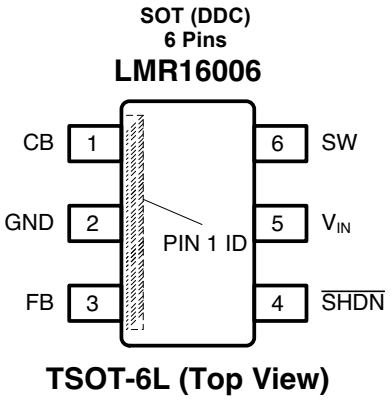
5 Revision History

DATE	REVISION	NOTES
October 2014	*	Initial release.

6 Pin Configuration and Functions



TSOT-6L (Top View)

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CB	1	I	Switch FET gate bias voltage. Connect C_{boot} cap between CB and SW.
GND	2	G	Ground connection.
FB	3	I	Feedback Input. Set feedback voltage divider ratio with $V_{OUT} = V_{FB}$ (1+(R1/R2)).
$\overline{SHDN}$	4	I	Enable and disable input (high voltage tolerant). Internal pull-up current source. Pull below 1.25 V to disable. Float to enable. Establish input undervoltage lockout with two resistor divider.
V_{IN}	5	I	Power input voltage pin. Input for internal supply and drain node input for internal high-side MOSFET.
SW	6	O	Switch node. Connect to inductor, diode, and C_{boot} cap.

7 Specifications

7.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
Input Voltages	V_{IN} to GND	-0.3	65	V
	$\overline{SHDN}$ to GND	-0.3	65	
	FB to GND	-0.3	7	
	CB to SW	-0.3	7	
Output Voltages	SW to GND	-0.3	65	
	SW to GND less than 30 ns transients	-2	65	
T_J Operation Junction temperature		-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-55	165	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)		500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Buck Regulator	V_{IN}	4	60	V
	CB	4	66	
	CB to SW	-0.3	6	
	SW	-0.3	60	
	FB	0	5.5	
Control	$\overline{SHDN}$	0	60	
Temperature	Operating junction temperature range, T_J	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)		SOT (6 PINS)	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance	102	°C/W
$R\theta_{JCtop}$	Junction-to-case (top) thermal resistance	36.9	
$R\theta_{JB}$	Junction-to board characterization parameter	28.4	

(1) All numbers apply for packages soldered directly onto a 3" x 3" PC board with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution, numberof thermal vias, board size, ambient temperature, and air flow.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = $\overline{SHDN}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} (Input Power Supply)						
V_{IN}	Operating input voltage		4		60	V
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V		1	3	µA
I_Q	Operating quiescent current (non-switching)	no load, V_{IN} = 12 V		28		µA
UVLO	Undervoltage lockout thresholds	Rising threshold			4	V
		Falling threshold	3			
$\overline{SHDN}$						
V_{SHDN_Thre}	Rising $\overline{SHDN}$ Threshold Voltage		1.05	1.25	1.38	V
I_{SHDN}	Input current	$\overline{SHDN}$ = 2.3 V		-4.2		µA
		$\overline{SHDN}$ = 0.9 V		-1		
I_{SHDN_HYS}	Hysteresis current			-3		µA
HIGH-SIDE MOSFET						
R_{DS_ON}	On-resistance	V_{IN} = 12 V, CB to SW = 5.8 V		900		mΩ
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage		0.747	0.765	0.782	V
CURRENT LIMIT						
I_{LIMIT}	Peak Current limit	V_{IN} = 12 V, T_J = 25°C		1200		mA
					1700	
THERMAL PERFORMANCE						
T_{SHDN} (1)	Thermal shutdown threshold			170		°C
T_{HYS} (1)	Hysteresis			10		°C

(1) Ensured by design

7.6 Switching Characteristics

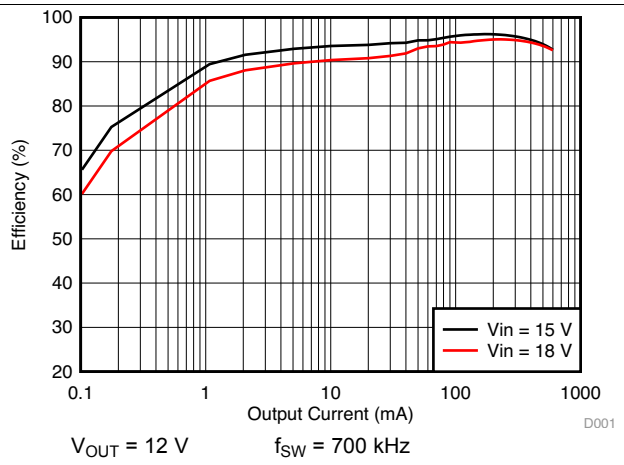
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW (SW PIN)						
f_{SW}	Switching frequency	LMR16006X	595	700	805	kHz
		LMR16006Y	1785	2100	2415	
T_{ON_MIN} (1)	Minimum turn-on time	f_{SW} = 2.1 MHz		80		ns
D_{MAX}	Maximum duty cycle	LMR16006X		96%		
		LMR16006Y		97%		

(1) Ensured by design.

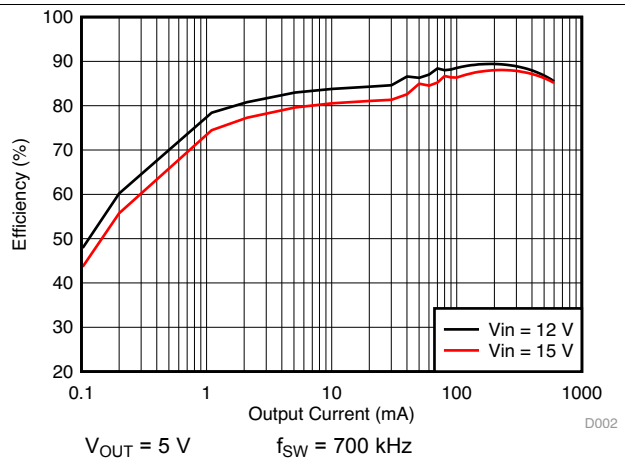
7.7 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 700 kHz, L1 = 22 µH, Cout = 10 µF, T_A = 25°C.



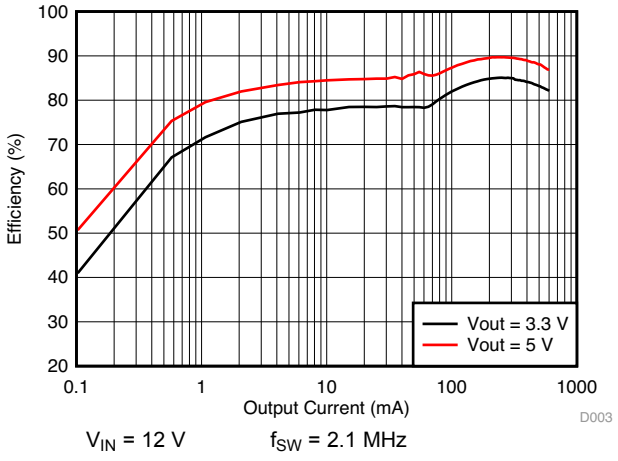
V_{OUT} = 12 V f_{SW} = 700 kHz

Figure 1. Efficiency vs. Load Current



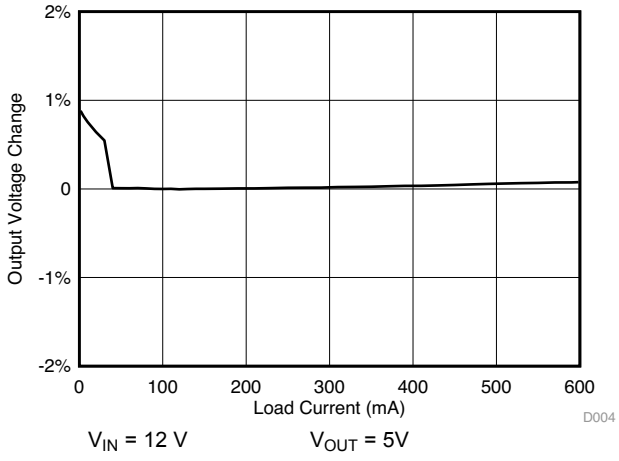
V_{OUT} = 5 V f_{SW} = 700 kHz

Figure 2. Efficiency vs. Load Current



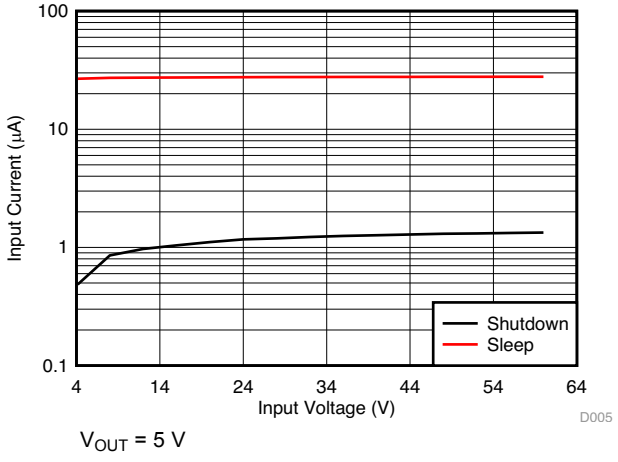
V_{IN} = 12 V f_{SW} = 2.1 MHz

Figure 3. Efficiency vs. Load Current



V_{IN} = 12 V V_{OUT} = 5V

Figure 4. Load Regulation



V_{OUT} = 5 V

Figure 5. Shut-Down Current and Quiescent Current

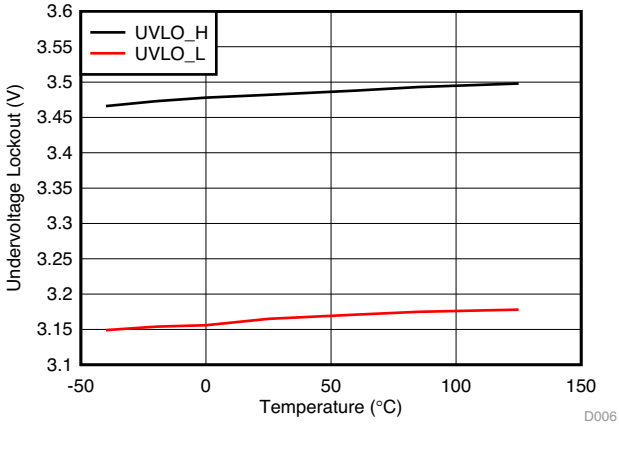


Figure 6. UVLO Threshold

Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 700 kHz, L1 = 22 µH, Cout = 10 µF, T_A = 25°C.

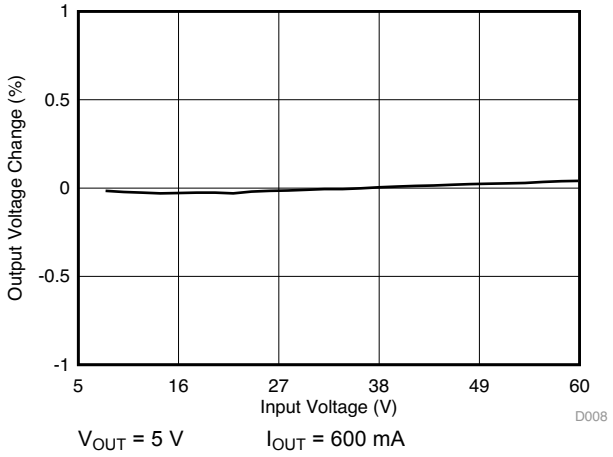


Figure 7. Line Regulation

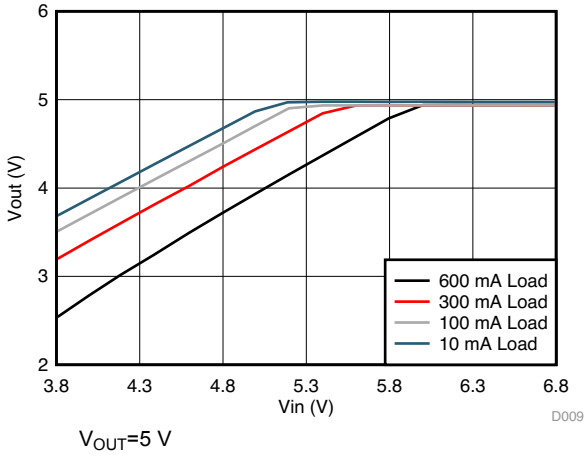


Figure 8. Dropout Curve

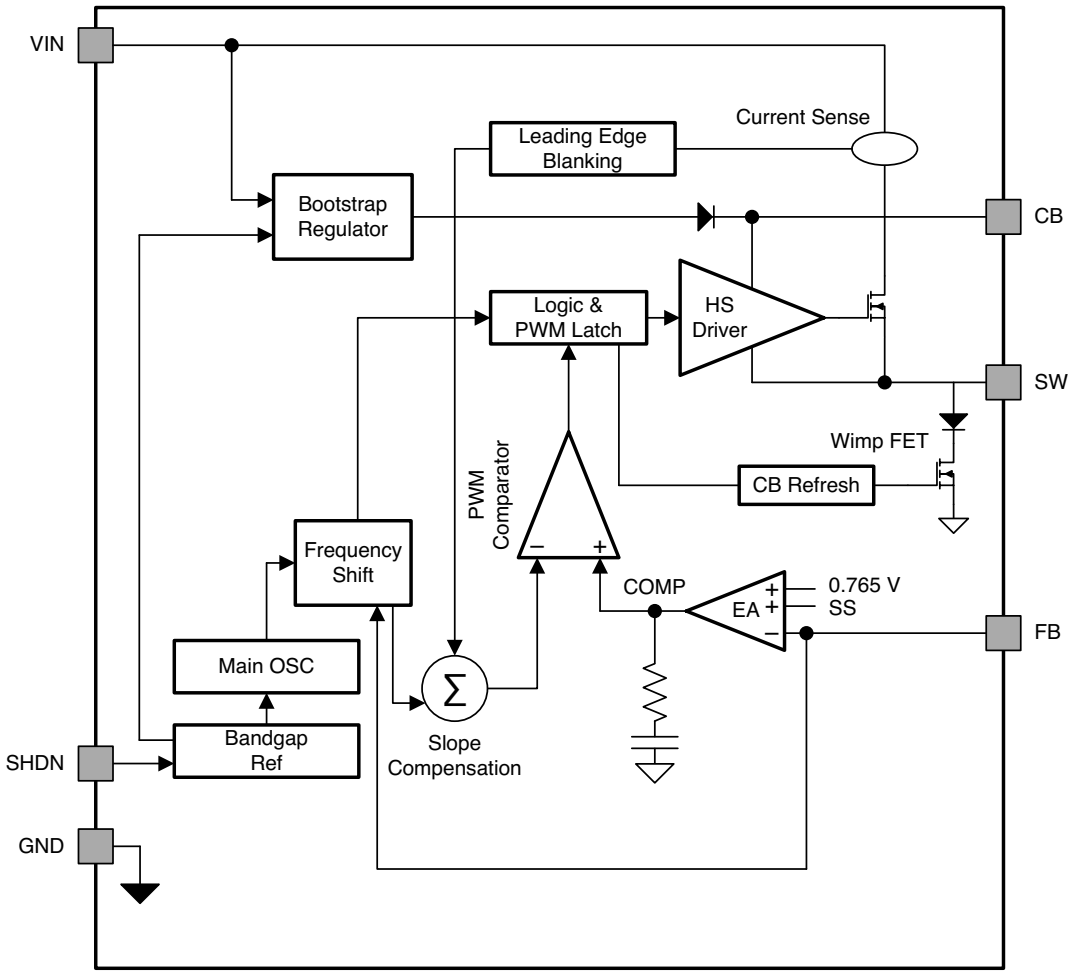
8 Detailed Description

8.1 Overview

The LMR16006 device is a 60 V, 600 mA, step-down (buck) regulator. The buck regulator has a very low quiescent current during light load to prolong battery life.

LMR16006 improves performance during line and load transients by implementing a constant frequency, current mode control which requires less output capacitance and simplifies frequency compensation design. Two switching frequency options, 0.7 MHz and 2.1 MHz, are available, thus smaller inductor and capacitor can be used. The LMR16006 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The LMR16006 can operate at high duty cycles because of the boot UVLO and refresh the wimp FET. The output voltage can be stepped down to as low as the 0.8 V reference. Internal soft-start is featured to minimize inrush currents.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The LMR16006 has two fixed frequency options, and it implements peak current mode control. The output voltage is compared through external resistors on the V_{FB} pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

8.3.2 Bootstrap Voltage (CB)

The LMR16006 has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high side MOSFET. The CB capacitor is refreshed when the high side MOSFET is off and the low side diode conducts. To improve drop out, the LMR16006 is designed to operate at 100% duty cycle as long as the CB to SW pin voltage is greater than 3 V. When the voltage from CB to SW drops below 3 V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the CB capacitor. Since the supply current sourced from the CB capacitor is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high. Attention must be taken in maximum duty cycle applications with light load. To ensure SW can be pulled to ground to refresh the CB capacitor, an internal circuit will charge the CB capacitor when the load is light or the device is working in dropout condition.

8.3.3 Output Voltage Setting

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage 0.765 V, so the ratio of the feedback resistors sets the output voltage according to the following equation: V_{OUT} = 0.765 V (1+(R1/R2)). Typically R2 will be given as 1k Ω - 100 kΩ for a starting value. To solve for R1 given R2 and Vout uses R1 = R2 ((V_{OUT}/0.765 V)-1).

8.3.4 Enable $\overline{\text{SHDN}}$ and VIN Undervoltage Lockout

LMR16006 $\overline{\text{SHDN}}$ pin is a high voltage tolerant input with an internal pull up circuit. The device can be enabled even if the $\overline{\text{SHDN}}$ pin is floating. The regulator can also be turned on using 1.23 V or higher logic signals. If the use of a higher voltage is desired due to system or other constraints, a 100 kΩ or larger resistor is recommended between the applied voltage and the $\overline{\text{SHDN}}$ pin to protect the device. When $\overline{\text{SHDN}}$ is pulled down to 0 V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode the supply current will be decreased to approximately 1 µA. If the shutdown function is not to be used the $\overline{\text{SHDN}}$ pin may be tied to V_{IN} via 100kΩ resistor. The maximum voltage to the $\overline{\text{SHDN}}$ pin should not exceed 60 V. LMR16006 has an internal UVLO circuit to shutdown the output if the input voltage falls below an internally fixed UVLO threshold level. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will power up when the input voltage exceeds the voltage level. If there is a requirement for a higher UVLO voltage, the $\overline{\text{SHDN}}$ can be used to adjust the system UVLO by using external resistors.

8.3.5 Current Limit

The LMR16006 implements current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and internal COMP voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

8.3.6 Overvoltage Transient Protection

The LMR16006 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier

Feature Description (continued)

output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 108% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

8.3.7 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C(typ). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C(typ), the device reinitiates the power up sequence.

8.4 Device Functional Modes

8.4.1 Continuous Conduction Mode

The LMR16006 steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at CCM), the buck regulator operates in two cycles. The power switch is connected between V_{IN} and SW. In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by Cout and the rising current through the inductor. During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as: $D = V_{OUT}/V_{IN}$ and $D' = (1-D)$ where D is the duty cycle of the switch, D and D' will be required for design calculations.

8.4.2 ECO Mode

The LMR16006 operates in ECO mode at light load currents to improve efficiency by reducing switching and gate drive losses. The LMR16006 is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the sleep current threshold, $I_{INDUCTOR} \leq 80$ mA, the device enters ECO mode. For ECO mode operation, the LMR16006 senses peak current, not average or load current, so the load current where the device enters ECO mode is dependent on V_{IN}, V_{OUT} and the output inductor value. When the load current is low and the output voltage is within regulation, the device enters an ECO mode and draws only 28 µA input quiescent current.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR16006 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 600 mA. The following design procedure can be used to select components for the LMR16006. This section presents a simplified discussion of the design process.

9.2 Typical Application

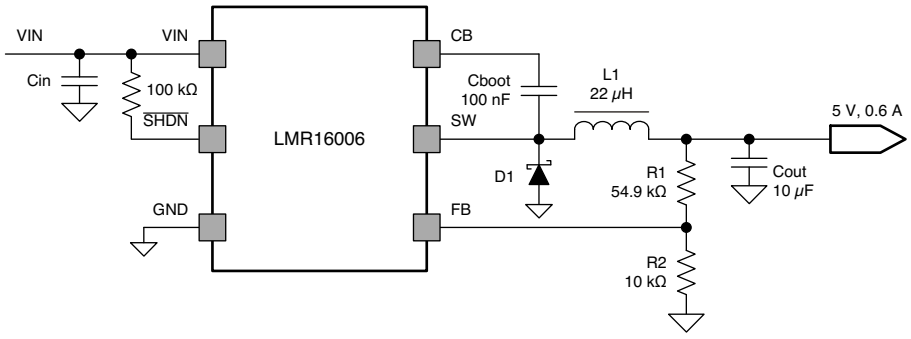


Figure 9. Application Circuit, 5 V Output

9.2.1 Design Requirements

Table 1. Design Example Parameters

Input Voltage, V_{IN}		9 V to 16 V, Typical 12 V
Output Voltage, V_{OUT}		5.0 V ± 3%
Maximum Output Current I_{O_max}		0.6 A
Minimum Output Current I_{O_min}		0.03 A
Transient Response 0.03 A to 0.6 A		5%
Output Voltage Ripple		1%
Switching Frequency Fsw		0.7 MHz
Target during Load Transient	Over Voltage Peak Value	106% of Output Voltage
	Under Voltage Value	91% of Output Voltage

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LMR16006 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance,

– Run thermal simulations to understand the thermal performance of your board,
– Export your customized schematic and layout into popular CAD formats,
– Print PDF reports for the design, and share your design with colleagues.

5. Get more information about WEBENCH tools at www.ti.com/webench.

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

9.2.2.2 Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. To calculate the minimum value of the output inductor, use Equation 1. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value is setting the ripple current to be 30%-40% of the DC output current. For this design example, the minimum inductor value is calculated to be 20.4 µH, and a nearest standard value was chosen: 22 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 3 and Equation 4. The inductor ripple current is 0.22 A, and the RMS current is 0.602 A. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. A good starting point for most applications is 22 µH with a 1.6 A current rating. Using a rating near 1.6 A will enable the LMR16006 to current limit without saturating the inductor. This is preferable to the LMR16006 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o\,\min} = \frac{V_{in\,\max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in\,\max} \times f_{sw}} \quad (1)$$

$$I_{ripple} = \frac{V_{out} \times (V_{in\,\max} - V_{out})}{V_{in\,\max} \times L_o \times f_{sw}} \quad (2)$$

$$I_{L\text{-}RMS} = \sqrt{I_o^2 + \frac{1}{12} I_{ripple}^2} \quad (3)$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \quad (4)$$

9.2.2.3 Output Capacitor Selection

The selection of Cout is mainly driven by three primary considerations. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 5 shows the minimum output capacitance necessary to accomplish this. The transient load response is specified as a 3% change in V_{OUT} for a load step from 0.03 A to 0.6 A (full load), ΔI_{OUT} = 0.6 -0.03 = 0.57 A and ΔV_{OUT} = 0.03 × 5 = 0.15 V. Using these numbers gives a minimum capacitance of 10.8 µF. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. Equation 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, Vf is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst case load step will be from 0.6 A to 0.03 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3% of the output voltage. This will make Vo_overshoot = 1.03 × 5 = 5.15 V. V_i is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 6 yields a minimum capacitance of 5.2 µF.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{sw} is the switching frequency, V_{o_ripple} is the maximum allowable output voltage ripple, and I_{L_ripple} is the inductor ripple current. Equation 7 yields 0.26 µF.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR should be less than 680 mΩ.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, 10 µF ceramic capacitors will be used. Capacitors in the range of 4.7 µF-100 µF are a good starting point with an ESR of 0.7 Ω or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{fsw \times \Delta V_{out}} \tag{5}$$

$$C_{out} > L_o \times \frac{(Ioh^2 - Iol^2)}{(Vf^2 - Vi^2)} \tag{6}$$

$$C_{out} > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{o\_ripple}}{I_{L\_ripple}}} \tag{7}$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L\_ripple}} \tag{8}$$

9.2.2.4 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. In the target application, the current rating for the diode should be equal or greater to the maximum output current for best reliability in most applications. In cases where the input voltage is not much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-D) × I_{OUT}. However the peak current rating should be higher than the maximum load current. A 0.5 A to 1 A rated diode is a good starting point.

9.2.2.5 Input Capacitor Selection

A low ESR ceramic capacitor is needed between the V_{IN} pin and ground pin. This capacitor prevents large switching voltage transients from appearing at the input. Use a 1 µF-10 µF value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor's value can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufactures data sheet for information on capacitor derating over voltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LMR16006. The input ripple current can be calculated using below Equation 9.

For this example design, one 2.2 µF, 50 V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, I_{OUT_max} = 0.6 A, Cin = 2.2 µF, f_{SW} = 700 kHz, yields an input voltage ripple of 97 mV and a rms input ripple current of 0.3 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\,\min}} \times \frac{(V_{in\,\min} - V_{out})}{V_{in\,\min}}} \tag{9}$$

$$\Delta V_{in} = \frac{I_{out\,\max} \times 0.25}{C_{in} \times fsw} \tag{10}$$

9.2.2.6 Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor or larger is recommended for the bootstrap capacitor (C_{BOOT}). For applications where the input voltage is close to output voltage a larger capacitor is recommended, generally 0.1 μF to 1 μF to ensure plenty of gate drive for the internal switches and a consistently low R_{DSON}. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

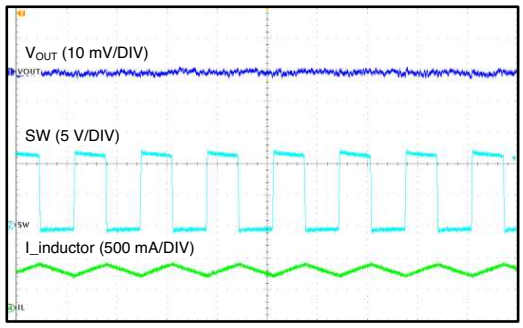
Table 2 represents the recommended typical output voltage inductor/capacitor combinations for optimized total solution size.

Table 2. Recommended Typical Output Voltage

P/N	Vout (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	Cout (μF)
LMR16006 Y	5	54.9 (1%)	10 (1%)	6.8	10
LMR16006 Y	12	147 (1%)	10 (1%)	10	10

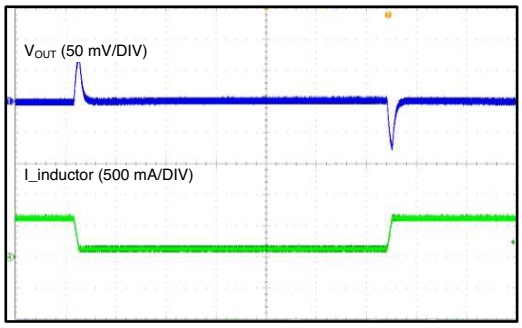
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 700 kHz, L1 = 22 µH, Cout = 10 µF, T_A = 25°C



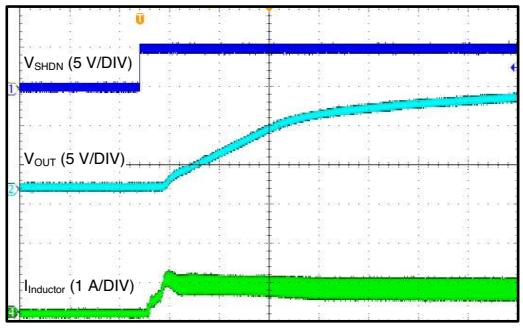
V_{OUT} = 5 V I_{OUT} = 600 mA

Figure 10. Output Voltage Ripple



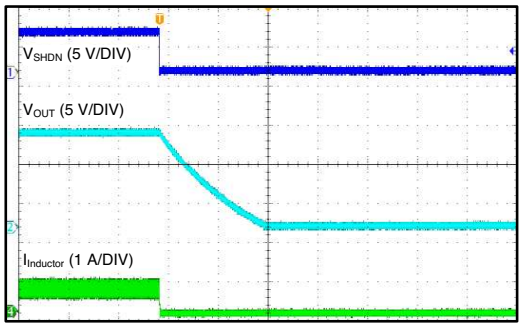
V_{OUT} = 5 V

Figure 11. Load Transient from 0.1 A to 0.6 A



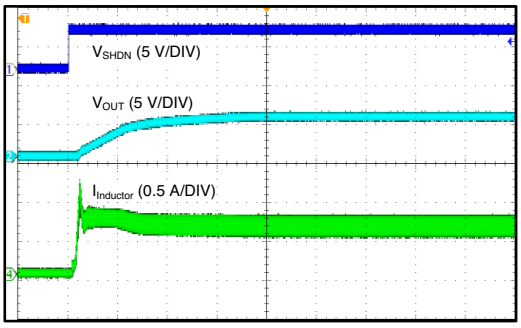
V_{IN} = 24 V V_{OUT} = 12 V I_{OUT} = 600 mA

Figure 12. Start-Up



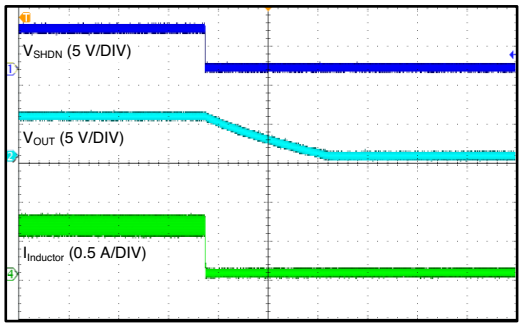
V_{IN} = 24 V V_{OUT} = 12 V I_{OUT} = 600 mA

Figure 13. Shut-Down



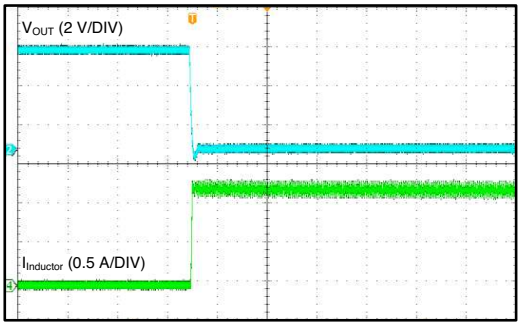
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 600 mA

Figure 14. Start-Up



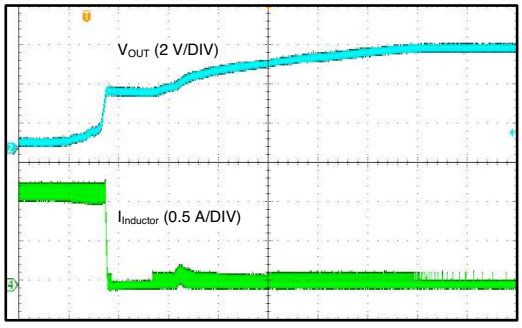
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 600 mA

Figure 15. Shut-Down



V_{IN} = 12 V V_{OUT} = 5 V

Figure 16. Short Circuit Entry



V_{IN} = 12 V V_{OUT} = 5 V

Figure 17. Short Circuit Recovery

10 Power Supply Recommendations

The LMR16006 is designed to operate from an input voltage supply range between 4 V and 60 V. This input supply should be able to withstand the maximum input current and maintain a voltage above 4 V. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMR16006 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR16006, additional bulk capacitance may be required in addition to the ceramic input capacitors.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin.
2. The input bypass capacitor Cin must be placed close to the V_{IN} pin. This will reduce copper trace resistance which effects input voltage ripple of the IC.
3. The inductor L1 should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, Cout should be placed close to the junction of L1 and the diode D1. The L1, D1, and Cout trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for the diode, Cin, and Cout should be as small as possible and tied to the system ground plane in only one spot (preferably at the Cout ground point) to minimize conducted noise in the system ground plane.
6. For more detail on switching power supply layout considerations see AN-1149 Layout Guidelines for Switching Power Supplies SNVA021

11.2 Layout Example

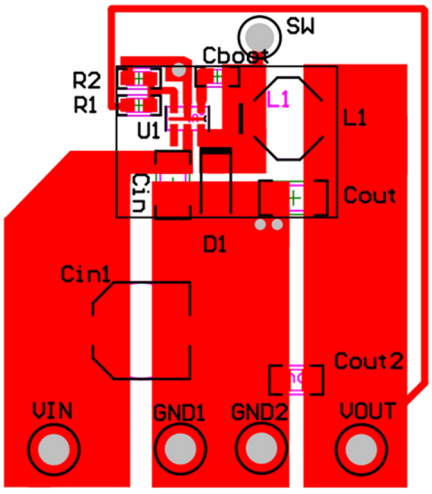


Figure 18. Layout

12 Device and Documentation Support

12.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LMR16006 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Related Documentation

AN-1149 Layout Guidelines for Switching Power Supplies SNVA021

12.4 Trademarks

WEBENCH is a registered trademark of Texas Instruments.
SIMPLE SWITCHER is a registered trademark of TI .
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR16006XDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D02X	Samples
LMR16006XDDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D02X	Samples
LMR16006YDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D02Y	Samples
LMR16006YDDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D02Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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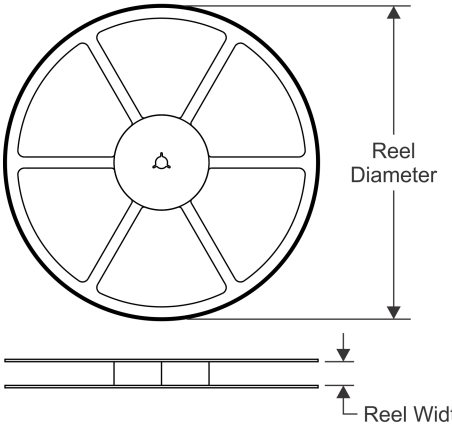
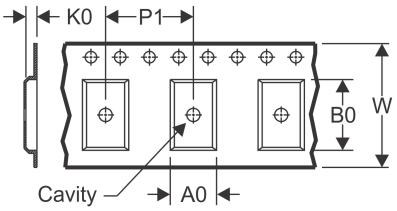
TAPE AND REEL INFORMATION

REEL DIMENSIONS

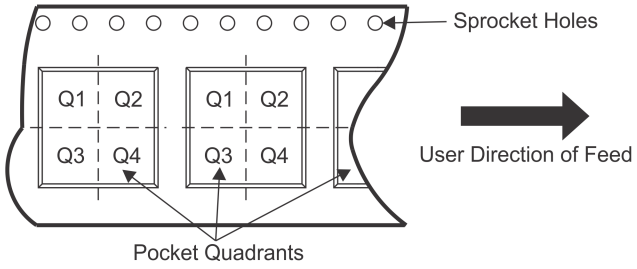


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

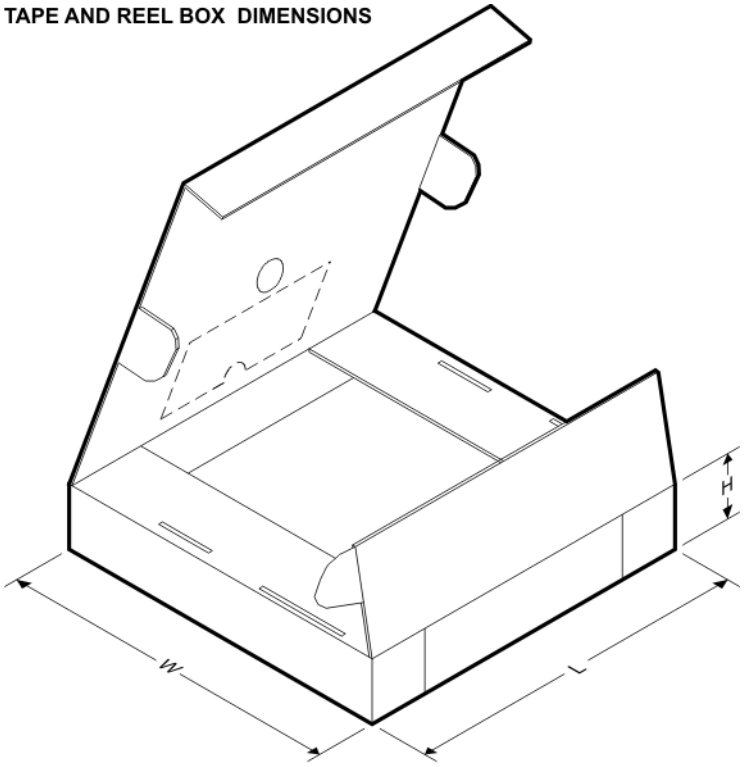
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR16006XDDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006XDDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006YDDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006YDDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

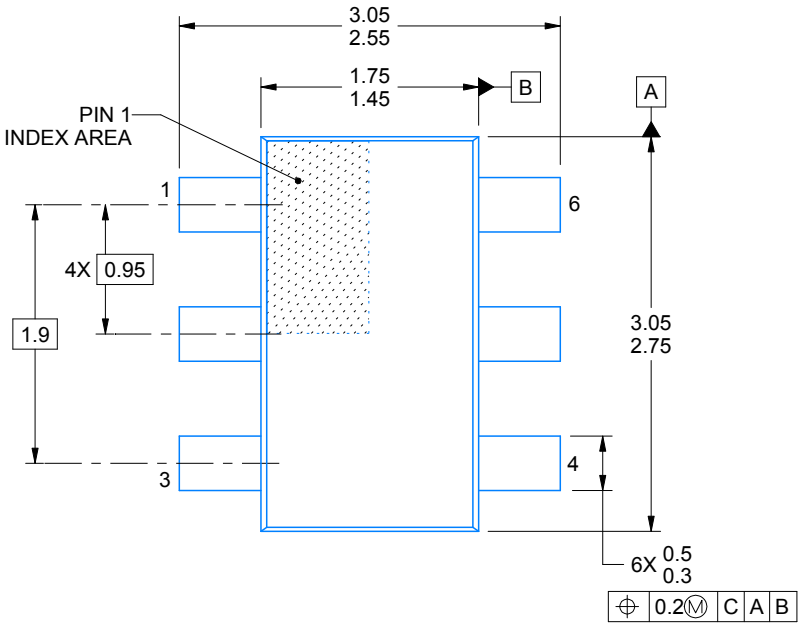
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR16006XDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR16006XDDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMR16006YDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR16006YDDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

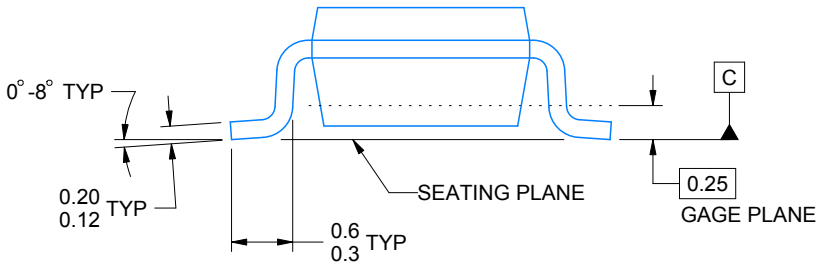
PACKAGE OUTLINE

DDC0006A

SOT - 1.1 max height

SOT





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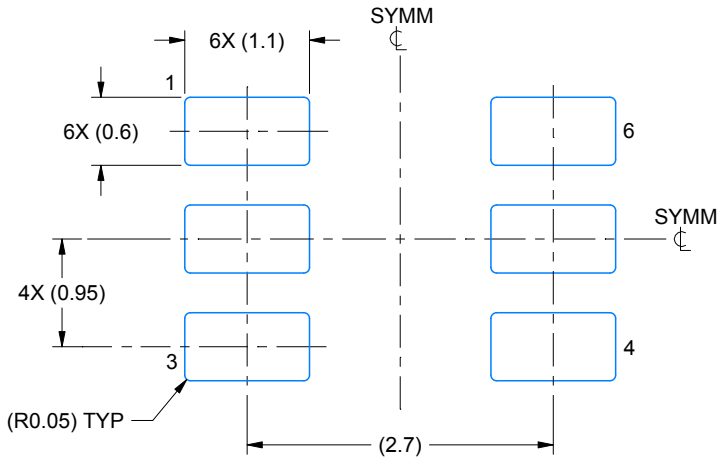
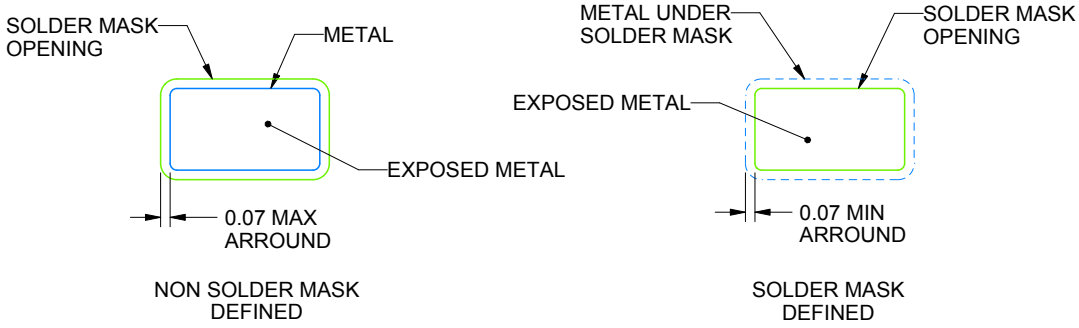
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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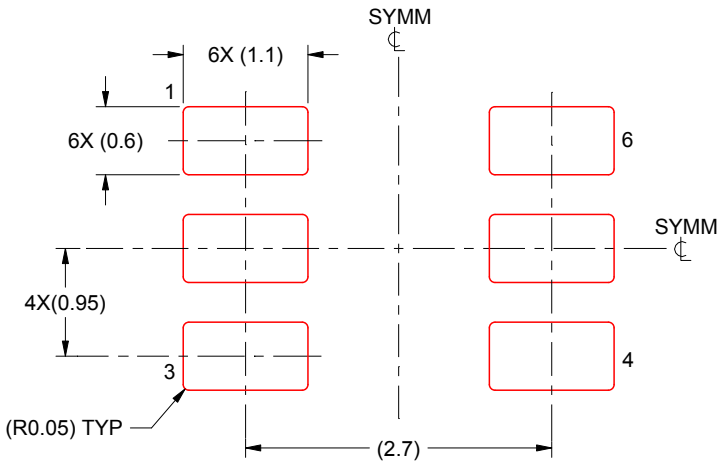
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/B 11/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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